Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (withdrawn). A method of producing a blank having a plurality of component positions for electronic components, the method which comprises the following method steps:

producing at least one of a carrier plate and a first plastic layer from a plastic compound being more highly crosslinked in a lower region than in an upper region;

fitting a semiconductor chip in each of the component positions of the blank with a passive surface of the semiconductor chip embedded in the first plastic layer, and thereby forming a bead of plastic compound of the first plastic layer, the bead surrounding marginal sides of the semiconductor chip up to a partial height thereof;

applying a second plastic layer, the first plastic layer having an upper boundary to the second plastic layer, the second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

forming a further component plane defined above the second plastic layer, and the second plastic layer having a level upper side forming an interface to the further component plane;

forming wiring structures with through-contacts between contact regions of the semiconductor chips and external contacts of electronic components disposed above at least one of the second plastic layer and the semiconductor chips; and

curing the plastic layers for forming a self-supporting, dimensionally stable plastic plate with embedded semiconductor chips in the component positions.

Claim 2 (withdrawn). The method according to claim 1, wherein the step of producing the carrier plate comprises coating a base plate heated to a temperature between 120 and 350°C with the first plastic layer of a plastic compound that, when the carrier plate with the first plastic layer is cooled down, defines a degree of crosslinking decreasing toward an upper boundary layer of the first plastic layer.

Claim 3 (withdrawn). The method according to claim 1, wherein the carrier plate is produced from a solid plastic, and the step of producing the carrier plate comprises subjecting the

first plastic layer of uncrosslinked plastic embedding compound to a temperature gradient, to partly crosslink the plastic embedding compound with a degree of crosslinking of the compound decreasing toward an upper boundary of the first plastic layer, and to form a first, substantially completely crosslinked, self-supporting, dimensionally stable lower region toward an underside in the first plastic layer.

Claim 4 (withdrawn). The method according to claim 1, which comprises providing an uncrosslinked plastic embedding compound for producing the first plastic layer filled with spherical particles of uniform sphere diameter.

Claim 5 (withdrawn). The method according to claim 4, wherein the spherical particles are glass spheres.

Claim 6 (withdrawn). The method according to claim 1, wherein the fitting step comprises initially pressing the semiconductor chip with an active upper side and the contact regions arranged thereon into the first plastic layer, forming the bead of plastic compound of the first plastic layer, the bead surrounding the marginal sides of the semiconductor chip, until the contact regions contact a metal carrier plate, and subsequently covering the passive rear side of the semiconductor chip with the second plastic layer.

Claim 7 (withdrawn). The method according to claim 1, wherein the fitting step comprises initially pressing the semiconductor chip with a passive side thereof into the first plastic layer, forming the bead of plastic compound of the first plastic layer, the bead surrounding the marginal sides of the semiconductor chip, and subsequently leveling the blank with the second plastic layer and leaving free at least contact regions of the semiconductor chip.

Claim 8 (withdrawn). The method according to claim 7, which comprises leaving free an entire active upper side of the semiconductor chip.

Claim 9 (withdrawn). The method according to claim 1, which comprises, following the step of applying the second plastic layer, completely crosslinking the plastic compounds of the plastic layers by heating.

Claim 10 (withdrawn). The method according to claim 1, which comprises, following the step of fitting the semiconductor chip into the first plastic layer in the component position of the blank, completely crosslinking the first plastic layer by heating.

Claim 11 (withdrawn). The method according to claim 1, which comprises applying the second plastic layer to a completely crosslinked first plastic layer with a transfer molding process.

Claim 12 (withdrawn). The method according to claim 1, which comprises applying the second plastic layer to a completely crosslinked first plastic layer with a spin-casting process.

Claim 13 (withdrawn). The method according to claim 1, which comprises curing the second plastic layer by heating the blank to a temperature of between 120 and 350°C for 2 to 30 minutes.

Claim 14 (withdrawn). The method according to claim 1, which comprises curing the second plastic layer by irradiating the blank with UV light.

Claim 15 (withdrawn). The method according to claim 14, which comprises irradiating for a duration ranging from a few seconds to a few minutes.

Claim 16 (withdrawn). The method according to claim 1, wherein the semiconductor chip is formed with contact regions, and the method comprises placing a wiring structure, for electrically connecting to the contact regions in the

semiconductor chip, to the self-supporting, dimensionally stable plastic plate in each component position.

Claim 17 (withdrawn). The method according to claim 1, which comprises exposing contact regions of the semiconductor chips of a blank with a photolithographic step.

Claim 18 (withdrawn). The method according to claim 16, wherein the step of placing the wiring structure comprises chemically or electrochemically depositing a metal.

Claim 19 (withdrawn). The method according to claim 16, wherein the step of placing the wiring structure comprises a three-stage electrochemical deposition process, including, first depositing a closed metal layer by sputtering, subsequently applying a photoresist mask in a pattern of the wiring structure, leaving the sputtered layer free, and, finally, electrochemically depositing metal on the structure having been left free, forming the wiring structure, and removing the photoresist layer and the sputtered layer following the formation of the wiring structure.

Claim 20 (withdrawn). The method according to claim 16, wherein the step of placing the wiring structure comprises

printing the wiring structure on the plastic plate in each component position.

Claim 21 (withdrawn). The method according to claim 16, which comprises forming further wiring layers on the plastic plate, by alternately arranging insulating layers with through-contacts and insulating layers with wiring lines on the at least one wiring structure.

Claim 22 (withdrawn). The method according to claim 1, which comprises fitting external contacts to an external wiring layer of the blank.

Claim 23 (withdrawn). A method of producing an electronic component, which comprises:

producing a blank in accordance with the method of claim 1; and

separating portions of the blank at component positions to form individual electronic components.

Claim 24 (currently amended). An electronic component with a semiconductor chip, comprising:

a multilayer plastic embedding compound embedding the semiconductor chip, said multilayer compound forming a first plastic layer and a second plastic layer;

the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

said first plastic layer having a bead surrounding the semiconductor chip;

said first plastic layer having a upper boundary adjoining said second plastic layer located thereabove;

said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

said second plastic layer having a level upper side forming a boundary interface to at least one further component plane; and

at least one wiring structure disposed above said second plastic layer, said wiring structure having through-contacts

between contact regions of the semiconductor chip and external contacts of the electronic component.

Claim 25 (original). The electronic component according to claim 24, wherein said first plastic layer is formed with a plastic embedding compound having different levels of crosslinking staggered vertically, with a highest level of crosslinking being arranged in a region of a base surface of said first plastic layer.

Claim 26 (original). The electronic component according to claim 24, wherein said first plastic layer is formed with a plastic embedding compound having a completely crosslinked region at a base plate and a precrosslinked region thereabove.

Claim 27 (original). The electronic component according to claim 24, which comprises spherical particles in said first plastic layer, said spherical particles forming spacers for the semiconductor chips in the first plastic layer and having a uniform predefined diameter.

Claim 28 (original). The electronic component according to claim 27, wherein said spherical particles are glass beads.

Claim 29 (original). The electronic component according to claim 24, wherein said second plastic layer has a polyimide resin forming a leveling compensating compound.

Claim 30 (cancelled).

Claim 31 (currently amended). ~~The electronic component according to claim 24, wherein the semiconductor chip has an active upper side embedded in said first plastic layer, and the semiconductor chip has passive rear sides covered by said second plastic layer~~ An electronic component with a semiconductor chip, comprising:

a multilayer plastic embedding compound embedding the semiconductor chip, said multilayer compound forming a first plastic layer and a second plastic layer;

the semiconductor chip having an active surface and a passive surface, the active surface being embedded in said first plastic layer;

the semiconductor chip having marginal sides surrounded, up to a partial height thereof, by said first plastic layer;

said first plastic layer having a bead surrounding the semiconductor chip;

said first plastic layer having an upper boundary adjoining said second plastic layer located thereabove;

said second plastic layer resting on regions of the marginal sides of the semiconductor chip not covered by said first plastic layer;

said second plastic layer having a level upper side forming a boundary interface to at least one further component plane; and

at least one wiring structure disposed above said second plastic layer, said wiring structure having through-contacts between contact regions of the semiconductor chip and external contacts of the electronic component.

Claim 32 (currently amended). The electronic component according to claim 24, wherein the active surface of the semiconductor chip ~~has an active upper side projecting~~ projects from said first plastic layer~~, and a passive rear side embedded in said first plastic layer~~.

Claim 33 (currently amended). A blank with a plurality of component positions for electronic components, each having at least one semiconductor chip, the blank comprising:

a first plastic layer surrounding the semiconductor chips on marginal sides and up to a partial height thereof;

a second plastic layer above said first plastic layer, said first plastic layer having a upper boundary to said second plastic layer;

the semiconductor chip having an active surface and a passive surface, the passive surface being embedded in said first plastic layer;

said first plastic layer having a bead surrounding the semiconductor chip;

said second plastic layer resting on regions of the marginal sides of the semiconductor chips not covered by said first plastic layer;

a further component plane defined above said second plastic layer, and said second plastic layer having a level upper side forming an interface to said further component plane;

wiring structures with through-contacts between contact regions of the semiconductor chips and external contacts of electronic components disposed above at least one of said second plastic layer and the semiconductor chips;

at least one of said first and second plastic layers being at least partly cured and forming a self-supporting, substantially dimensionally stable, multilayer plastic plate.

Claim 34 (original). The blank according to claim 33, wherein said first plastic layer is formed with a plastic embedding compound having different levels of crosslinking staggered vertically, with a highest level of crosslinking being arranged in a region of a base surface of said first plastic layer.

Claim 35 (original). The blank according to claim 33, wherein said first plastic layer is formed with a plastic embedding compound having a completely crosslinked region at a base plate and a precrosslinked region thereabove.

Claim 36 (original). The blank according to claim 33, which comprises spherical particles in said first plastic layer, said spherical particles forming spacers for the semiconductor

chips in the first plastic layer and having a uniform predefined diameter.

Claim 37 (original). The blank according to claim 36, wherein said spherical particles are glass beads.

Claim 38 (original). The blank according to claim 33, wherein said second plastic layer has a polyimide resin forming a leveling compensating compound.

Claim 39 (original). The blank according to claim 33, wherein said wiring structure has an adhesive layer on interfaces to a plastic plate formed by said first and second layers.

Claim 40 (currently amended). A blank with a plurality of component positions for electronic components, each having at least one semiconductor chip, the blank comprising:

a first plastic layer surrounding the semiconductor chips on marginal sides and up to a partial height thereof;

a second plastic layer above said first plastic layer, said first plastic layer having an upper boundary to said second plastic layer;

the semiconductor chip having an active surface and a passive surface, the active surface being embedded in said first plastic layer;

said first plastic layer having a bead surrounding the semiconductor chip;

said second plastic layer resting on regions of the marginal sides of the semiconductor chips not covered by said first plastic layer;

a further component plane defined above said second plastic layer, and said second plastic layer having a level upper side forming an interface to said further component plane;

wiring structures with through-contacts between contact regions of the semiconductor chips and external contacts of electronic components disposed above at least one of said second plastic layer and the semiconductor chips;

at least one of said first and second plastic layers being at least partly cured and forming a self-supporting, substantially dimensionally stable, multilayer plastic plate

~~The blank according to claim 33, wherein the semiconductor chip has an active upper side embedded in said first plastic layer, and the semiconductor chip has passive rear sides covered by said second plastic layer~~.

Claim 41 (currently amended). The blank according to claim 33, wherein the active surface of the semiconductor chip ~~has an active upper side projecting~~ projects from said first plastic layer~~, and a passive rear side embedded in said first plastic layer~~.